POWERMASTER SEMICONDUCTOR

Masters of Power Solution

Consideration on Output Capacitance of a Power MOSFETs in Hard and Soft Switching Topologies

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1. Introduction

Although the efficiency of power supplies has improved significantly, most efforts focus on improving efficiency at medium to heavy loads. However, light-load efficiency is becoming more and more important. For example, the 80-Plus Titanium efficiency standards not only require 96% efficiency at a 50% load, but 90% efficiency at a 10% load and 94% efficiency at a 20% load. Maintaining high efficiency at light-load conditions is extremely important in most electronic and electrical appliances, where the digital loads spend the majority of their time in idle mode. Server applications that require highly reliable power sources will employ a redundant power supply system that is comprised of two (or more) power-supply units. Each power supply works at a light load most of the time; therefore, light-load efficiency is more meaningful than heavy-load efficiency. In addition to, power conversion switching frequency is being continuously increased to maximize power density. Soft switching techniques such as zero voltage switching (ZVS) have become popular to extend the frequency further. As switching frequency increases, power MOSFET parasitic characteristics are not negligible anymore. Among all parasitic elements, an output capacitance is crucial parasitic parameter to set power converter design up in both hard switching and soft switching topologies. It determines how much inductance is required to provide ZVS conditions, how dead time can be reduced in soft switching topologies and how much efficiency is improved in hard and soft switching topologies. There are many parameters such as $C_{O(tr)}$, $C_{O(er)}$, Q_{OSS}, E_{OSS} and E_{Dyn} related to C_{OSS} of Power MOSFETs. . This application note describes definition of these parameters and how they affect to each topologies.

2. C_{OSS} of Power MOSFETs

MOSFET is consisted with 3 types of capacitances as shown in figure 1. C_{oss} is defined as “C = Capacitance, o = output, s = Source, s = Short”, the output capacitance is measured the capacitance between the drain to source at f = 250kHz. $C_{oss} = C_{gs}$ $((C_{gs} \cdot C_{gd}) / C_{gd} + C_{gs}) + C_{ds} \approx C_{gd} + C_{ds}$, output capacitance is summation of drain-gate capacitance and drain-source capacitance.

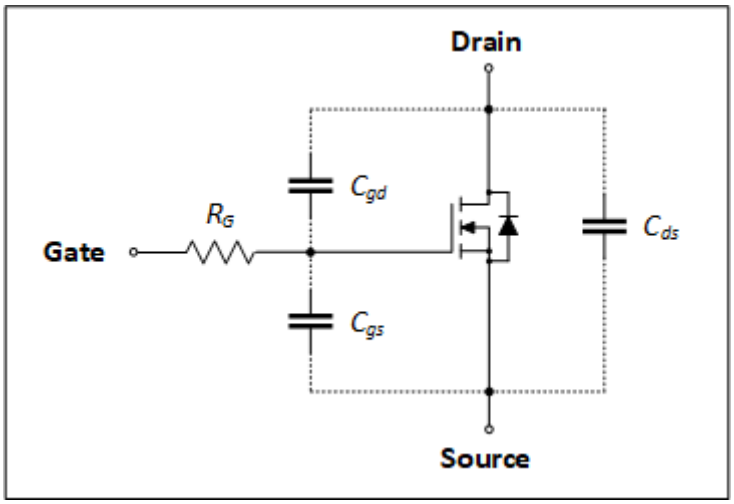

Figure 1. Equivalent Capacitance of Power MOSFET

Traditionally, many designers used rough assumptions to find out fixed value of output capacitance for the equations. This conventional equivalent output capacitance value, however, is not too helpful in real applications because it is varied by drain-source voltage and does not provide stored energy information accurately during switching on/off

transition. According to precedence, MOSFET datasheets show output capacitance at a single voltage as shown in table 1. While these values were good enough for relative comparison between products in the past, it is misleading to use these values for modern devices. A better representation of product capacitance is needed.

Table 1. Capacitances of 600V MOSFET at Single Voltage (V_{DS}=400V) in datasheet

C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 250 kHz		1240		pF
C_{oss}	Output Capacitance			34		pF
$C_{o(tr)}$	Time Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		381		pF
$C_{o(er)}$	Energy Related Output Capacitance			54		pF

As shown in figure 2 the output capacitance of a MOSFET is drain-source voltage dependent; therefore a single point measurement does not accurately represent the capacitance characteristic of the device. Curve fitting can be used to find an output capacitance equation from this single point.

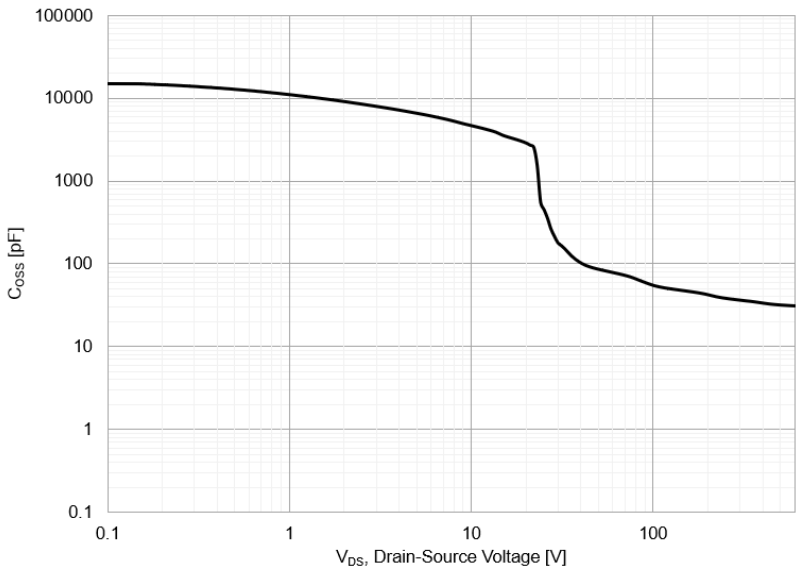

Figure 2. C_{OSS} Curve of 600V MOSFET according to Drain-Source Voltage (V_{DS})

Equation 1 below is an example based on capacitance at 25 V. This formula's integral could then be used in place of a single value capacitance in applicable equations. Equation 1 worked fairly well for planar devices, however more complex structures, like super-junction, are poorly represented leading to excessive error in any calculations due to non-linear C_{OSS} characteristic of super-junction MOSFETs. Rather than creating a different equation to better fit the capacitance characteristic of each new device architecture, effective capacitance measurements can be used. Effective capacitance values represent the capacitance that results in the same charge time or charge energy up to a given voltage. These values take the change of capacitance into account without the need for complex formulas or integration like would be required when using Equation 1.

Equation 1)

$$C_{OSS}(V_{DS}) = C_{OSS}(25V) \cdot \sqrt{\frac{25V}{V_{DS}}}$$

3. Using Effective Capacitances

Effective capacitances can be used in modeling energy loss and designing resonant topologies. When modeling energy loss for hard switching topologies, the stored energy in the output capacitance is lost as heat every switching cycle. As the switching frequency increases, the switching losses increase in proportion to the switching frequency and it dramatically affects to system efficiency. The relationship of output capacitance to power loss is shown in equation 2. This is only one component of switching loss, but it is critical to consider. The additional power dissipation from switching needs to be taken into account when selecting a MOSFET and designing any heatsinking for the MOSFET.

Equation 2)

$$P_{COSS} \approx \frac{1}{2} \cdot C_{OSS\_eff} \cdot V_{DS}^2 \cdot \mathrm{f}$$

In resonant topologies the effective capacitance is used to ensure zero voltage switching (ZVS). Zero voltage turn-on is achieved by using the stored energy in inductor, the leakage and series inductance or magnetizing inductance of the transformer, to discharge the output capacitance of the switches through resonant action. The inductance should be precisely designed to prevent hard switching that causes additional power losses. The output capacitance of the switches plays important role in both equation 3 and 4. To achieve ZVS, the magnetizing current and dead time must be great enough to discharge the output capacitance of one MOSFET and charge another. If the inductive energy is too small, the circuit will operate in hard switching mode, losing some of the efficiency gained by changing to a resonant topology. If the inductive energy is too large, excess energy will be lost, again minimizing the efficiency gained through the using of a resonant topology. In order to design the resonant circuit such that the inductive energy is as low as possible while still maintaining ZVS, the effective capacitance of the MOSFET must be used, as in equation 3 and 4. Therefore, obtaining exact output capacitance of the switches is very critical to optimum design of the soft switching converters.

The following equations are basic requirements for zero voltage switching.

Equation 3)

$$\text{Inductive Energy} \geq \text{Capacitive Energy}$$

$$\frac{1}{2} \cdot \mathrm{L}_{eq} \cdot I_L^2 \geq \frac{1}{2} \cdot (2 \cdot C_{OSS_{eff}}) \cdot V_{DS}^2$$

The effective capacitance is also needed to calculate dead time, Δt in equation 4.

Equation 4)

$$\Delta t \geq \frac{2 \cdot C_{OSS\_eff} \cdot V_{DS}}{I_{Magnetizing}}$$

3.1. Time Related Output Capacitance, $C_{o(tr)}$ and Energy Related Output Capacitance, $C_{o(er)}$

There are two equivalent fixed capacitances for the output capacitance C_{OSS}.

Table 1. $C_{o(tr)}$ and $C_{o(er)}$: Effective Output Capacitances of MOSFET

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$C_{o(tr)}$	Time Related Output Capacitance	V_{DS} = 0V ~ 400V, V_{GS} = 0V		381		pF
$C_{o(er)}$	Energy Related Output Capacitance			54		pF

$C_{o(tr)}$ is defined as “C = Capacitance, o = Output, tr = Time Related”, $C_{o(tr)}$ is a kind of time dominant capacitance which is the same charging time as the output capacitance of a MOSFET under V_{DS} is rising from zero voltage to 400V at V_{GS} = 0V. The time related output capacitance is call as “effective output capacitance”. $C_{o(tr)}$ is calculated as equation 5 and 6. For dead time calculation, it is important to know that in how much time the output capacitance will charge, and dead time should be kept higher than that 'tr' time.

Equation 5) V_{DS}: the voltage of drain to source by time dependent

$$V_{DS} = BV_{DSS}\left(1 - e^{-t_r/RC_{o(tr)}}\right)$$ *: t_r = rising time*

Equation 6) $C_{o(tr)}$: Calculation from Equation 7) at V_C = 400V

$$C_{o(tr)} = 6.21 \times 10^{-6} t_r$$

The method to measure the time related effective capacitance ($C_{o(tr)}$) is a totem pole driver, depicted in figure 3. This driver will charge the MOSFET to its rated drain voltage through a R_D while an oscilloscope monitors the drain voltage. The rise time (tr) of the drain to 80% of the rated BV_{DSS} is measured.

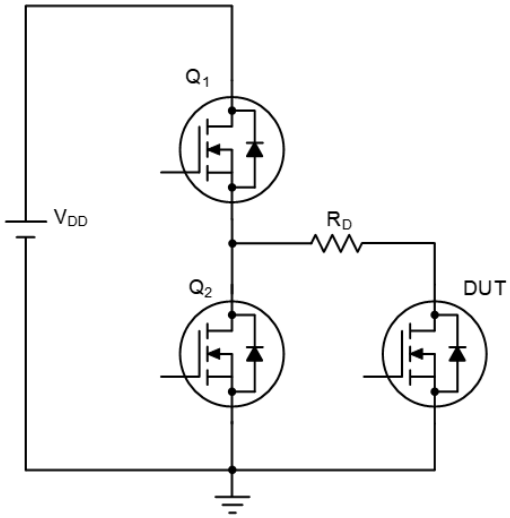

Figure 3. $C_{o(tr)}$ Test Circuit Utilizing a Totem Pole configuration

$C_{o(er)}$ is defined as “C = Capacitance, o = Output, er = Energy Related”, The energy related out capacitance is calculated from E_{OSS} to charging C_{OSS} in the MOSFET datasheet. $C_{o(er)}$ is useful to simulate the energy loss and design in resonant topologies such as LLC topology. To get the energy related effective capacitance $C_{o(er)}$, use the voltage dependent capacitance function in equation 7.

Equation 7) $C_{o(er)}$

$$C_{o(er)} = \frac{2}{{V_{DS}}^2}\int_0^{V_{DS}} C(v) \times v dv$$

$C_{o(tr)}$ is greater than $C_{o(er)}$, so it will be worth taking $C_{o(tr)}$ for calculation of dead time.

3.2. The stored energy in the output capacitance, E_{OSS}

The stored energy in the output capacitance of a MOSFET can be calculated by integrating the product of the output capacitance and drain-source voltage with respect to the drain-source voltage from zero to the drain-source voltage just before the turn-on transient. Figure 4 shows E_{oss} vs. Drain to Source Voltage, E_{OSS} is equivalent stored energy in output capacitance at V_{DS}=400V. E_{oss} is calculated as equation 8.

Equation 8) E_{OSS}: The cumulated energy to output capacitor by the voltage of the drain to source.

$$E_{oss} = \frac{1}{2}\left(C_{o(er)} \times {V_{DS}}^2 \right) = \int_0^{V_{DS}} C(v) \times v dv$$

C(v) is the capacitance by voltage as shown in figure 2.

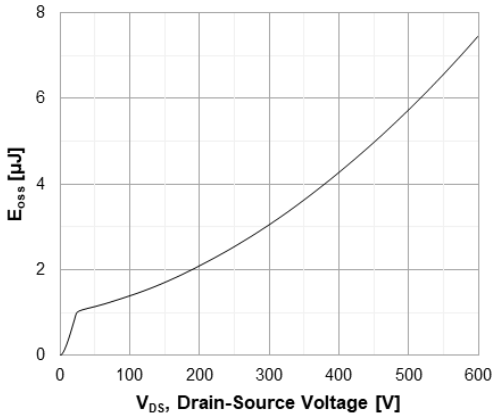

Figure 4. E_{oss} vs. Drain to Source Voltage

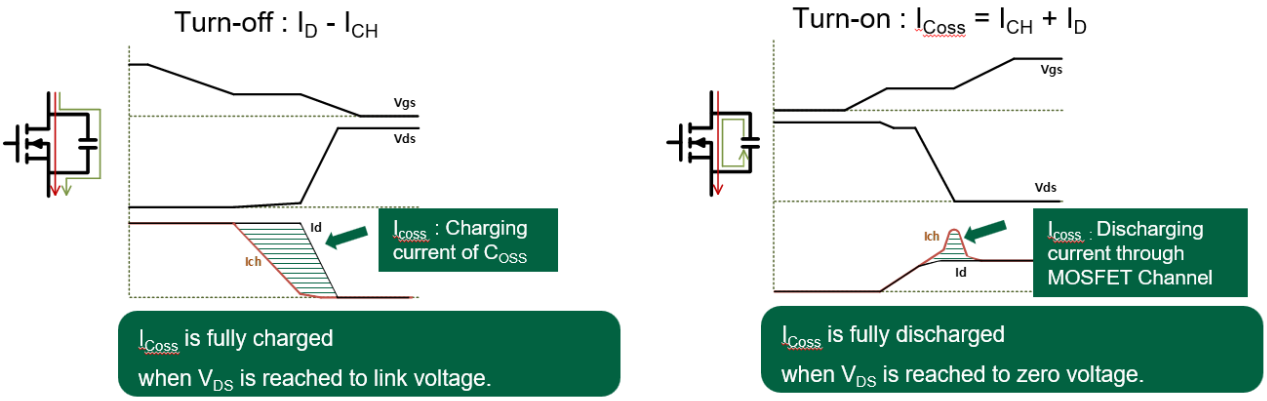

Figure 5. E_{OSS} dissipation Mechanism in during Turn-off and Turn-on transient in hard switching topology

Figure 5. clearly shows that the channel current (I_{ch}) is significantly lower than the drain current (I_D) during turn-off because drain current is diverted from the MOSFET channel to charge the output capacitor. At turn-on transient, The MOSFET channel conducts a current significantly higher than drain current (I_d) because of the additional current coming from the discharging of the output capacitor. The stored energy in the output capacitance of the power

MOSFET during turn-off is internally dissipated through the MOSFET channel in the form of joule heating during turn-on in hard switching topology. This stored energy is dissipated through the channel of the MOSFET on every turn-on of the switching cycle. As shown in figure 6, E_{oss} of the MOSFET, is very critical in hard-switching applications, such as flyback/forward converters or Power Factor Correction (PFC), especially at light loads and high switching frequency, because it is fixed and independent of load.

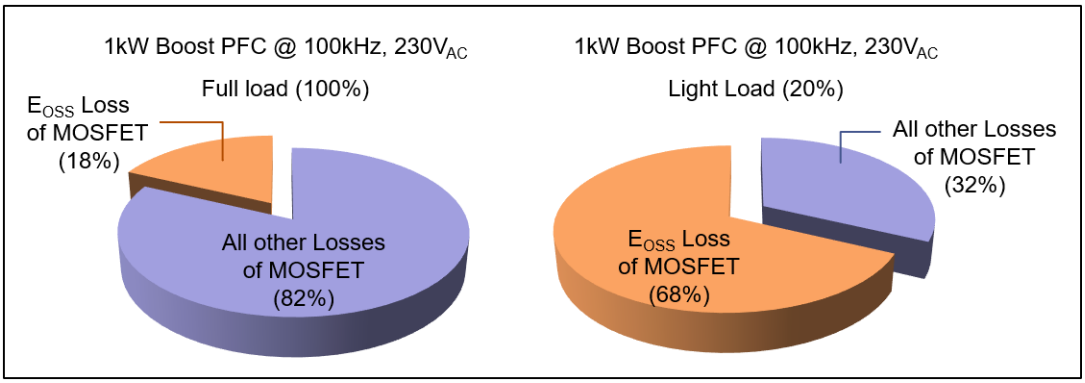

Figure 6. Power Loss Contribution of MOSFET in CCM PFC

3.3. The charge on the output capacitance Qoss

Q_{OSS} is the amount of charge for charging drain-source capacity. Figure 7 shows Q_{oss} vs. Drain to Source Voltage by calculating the area under the C_{OSS} curve. Q_{oss} is calculated as equation 11.

Equation 11) Q_{OSS}: The integral of the C_{OSS} along the voltage of the drain to source.

$$Q_{oss} = \int_0^{BV_{DSS}} C(v)\,\mathrm{dv}$$

C(v) is the capacitance by voltage as shown in figure 2

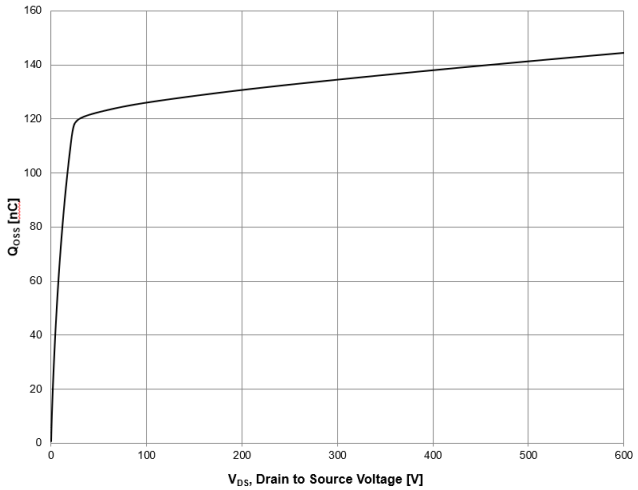

Figure 7. Q_{OSS} vs. Drain to Source Voltage

The reduction in Q_{OSS} is critical to achieve ZVS, the dead time between the high side and low side MOSFETs in the same leg must be long enough to allow the voltage transition. The time condition for achieving ZVS is given by equation

Equation 12) Dead time condition for ZVS

$$\text{dead time} \geq 2 \cdot \frac{Qoss}{I}$$

where I is the current used to charge and discharge both FETs in the leg

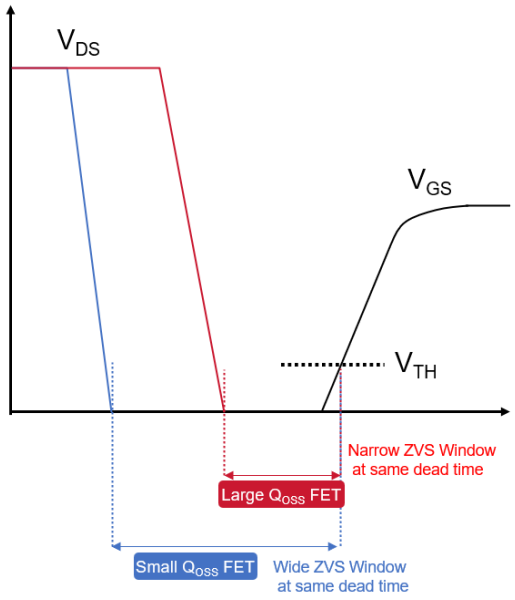

Figure 8. Dead time margin by Q_{OSS}

In resonant applications, Q_{OSS} is directly related to the charge which has to be provided and also the time needed to build up or release the reverse voltage. As shown in figure 8, MOSFETs that has smaller Q_{OSS} provide wider ZVS window at same dead time than that has larger Q_{OSS}. Therefore, circuit designer enables to increase switching frequency and losses for high power density with low Q_{OSS} devices.

3.4. The energy loss related dynamic C_{OSS}, E_{Dyn}

Recently, energy loss by dynamic C_{OSS} (E_{Dyn}) is analyzed in many papers. Unexpected power losses associated with the super junction MOSFETs in ZVS topologies generated. When the MOSFET C_{OSS} is charged and subsequently discharged some energy is lost due to the hysteretic phenomenon that the entire energy stored in the output capacitance (Eoss) is not recovered. Figure 9 shows electron current (black dot line) and hole current (red dot line) and charge pockets (resistance) during charge and discharge of super-junction MOSFET. Current flow of electrons and holes originates charges between N and P pillars that must be removed through a highly resistive path. The resistance by this charge pocket (R_{OSS}) can considered constant equivalent resistor during charging and discharging. This energy losses can be observed by hysteresis loop area large signal C_{OSS} during charge-discharge cycle as shown in figure 10. Therefore, dynamic C_{OSS} loss can be called as hysteresis C_{OSS} loss or R_{OSS} loss.

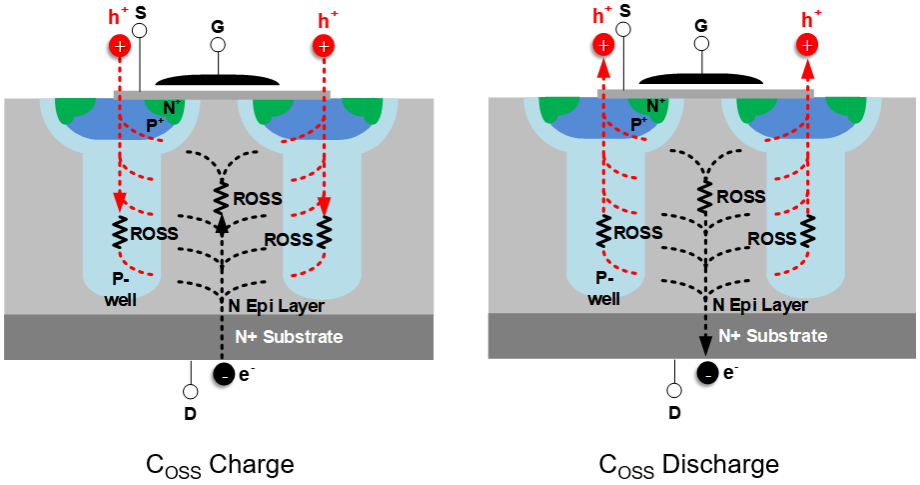

Figure 9. C_{OSS} charge and discharge of SJ MOSFET, Electron (e^-) (black dot line) and hole(h^+) currents (red dot line) and charge pockets

The energy loss (E_{Dyn}) related to dynamic C_{OSS} of the super-junction MOSFET depends on the design. A dynamic C_{OSS} loss (E_{Dyn}) generates for every switching cycle and increases the energy dissipated in the device. This E_{Dyn} is affected by device structure, die size, switching dV_{DS}/dt. Resonant converters are supposed to generate zero switching losses during soft switching operation, Dynamic C_{OSS} loss (E_{Dyn}) is highly impact on system efficiency especially, in resonant topologies at light load and high switching frequency operation.

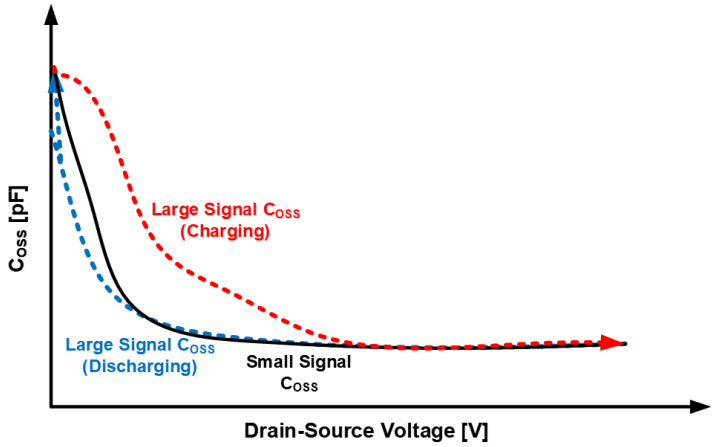

Figure 10. Comparison between small signal C_{OSS} (black line) and large signal C_{OSS}(red and blue lines)

4. Conclusion

The output capacitance of power semiconductor devices is important in determining the switching losses and in the operation of some resonant converter topologies. As operating frequency increases for high power density, the output capacitance of the MOSFET is playing an important role in efficiency and switching frequency. This application note provides understanding of how energy is consumed in the MOSFET's output capacitance during charging and discharging and how effective capacitances can be used in ZVS resonant topologies for designers.

5. Document Revision History

Major changes since the last version

Date	Description of change
15-December-2022	First Release

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